

In the specification:

Please change paragraph [Para 7] to:

- 5 [Para 7] Figure 2 is a multi-processor system with duplicate tags for coherency
snooping. Rather than ~~track-tracking~~ memory line coherency on a per-memory-line basis
in memory directory 12, the caches may themselves track cache-line coherency on a per-
cache-line basis. When a cache requests to write to a line, it broadcasts the line's address
to all other caches in the multi-processor system. The other caches compare the line's
10 address to tags in the local caches and invalidate the cache line if a tag matches.

Please change paragraph [Para 12] to:

- [Para 12] Figure 3 is a multi-processor system with a central location for duplicate
15 tags for coherency snooping. Rather than ~~have~~having duplicate tags with each cache, a
central snoop directory can store all duplicate tags. Cache line 24 in cache 14 has an entry
in central duplicate tags 40 that indicates that the cache line is present in cache 14, and
whether the line has been written (dirty). Likewise, cache line 26 in second cache 16 has
an entry in central duplicate tags 40. When a cache line exists in more than one cache,
20 entry 38 in central duplicate tags 40 can indicate which caches have the line, and which
copies have been written.

Please change paragraph [Para 14] to:

- 25 [Para 14] What is desired is a multi-processor system that can expand the number of
processors and local caches, while still providing cache-line coherency. Cache-line-based
base rather than memory-line-base coherency is desired to reduce the size of the
coherency directory.